WHAT IS CLAIMED IS;

1. A multi-layered semiconductor device characterized in that a film-like semiconductor package incorporating therein a semiconductor chip is disposed in a package accommodation opening of a circuit pattern layer to form a circuit board, and a plurality of such circuit boards are layered together to electrically connect circuit patterns of the respective circuit boards with each other.

2. A multi-layered semiconductor device as defined by claim 1, wherein every adjacent circuit board is bonded to another with an insulation adhesive except for an electrically connected portion.

3. A multi-layered semiconductor device as defined by claim 1, wherein the electrical connection between the circuit patterns on the respective circuit boards is performed via a low melting point metal filled in a through-hole formed in the semiconductor package or the circuit board.

4. A multi-layered semiconductor device as defined by claim 1, wherein the electrical connection between the circuit patterns on the respective circuit boards is performed by connecting an extension of the circuit pattern into a hole formed in the semiconductor package or the circuit board with an electrode pad of the circuit pattern in the other circuit board positioned beneath the former circuit board.

5. A multi-layered semiconductor device as defined by claim 1, wherein the electric connection between the semiconductor package and a circuit pattern layer accommodating the semiconductor package is performed by connecting an extension of the circuit pattern, formed on the semiconductor package to project outside the package, with an electrode pad of the circuit pattern layer.

6. A method for producing a multi-layered semiconductor device characterized in that the method comprises the steps of separately testing a film-like

semiconductor package including a semiconductor chip therein and a circuit pattern layer having an opening for accommodating the semiconductor package; forming a circuit board by disposing the semiconductor package in the opening of the circuit pattern layer; and superposing a plurality of the circuit boards together and electrically connecting the circuit patterns of the respective circuit boards with each other.

7. A method as defined by claim 6, wherein every adjacent circuit board is bonded to another with an insulation adhesive except for an electrically connected portion.

8. A method as defined by claim 6, wherein the electrical connection between the circuit patterns on the circuit boards is performed by filling a through-hole formed in the package or the circuit board with a low melting point metal.

9. A method as defined by claim 6, wherein the electrical connection between the circuit patterns on the circuit boards is performed by connecting an extension of the circuit pattern, into a hole formed in the semiconductor package or the circuit board, with an electrode pad of the circuit pattern on the other circuit board positioned beneath the former circuit board.

10. A method as defined by claim 6, wherein the electric connection between the semiconductor package and a circuit pattern layer accommodating the semiconductor package is performed by connecting an extension of the circuit pattern formed on the semiconductor package to project outside the package with an electrode pad of the circuit pattern layer.

11. A multi-layered semiconductor device formed of a plurality of circuit boards layered together, each circuit board comprising an insulation substrate, a semiconductor chip incorporated in the substrate, a circuit formed on a surface of the substrate and connected to the semiconductor chip, characterized in

that a lead extending from the circuit on the circuit board is bonded, in a through-hole provided in the insulation substrate of the circuit board, to a circuit on another circuit board disposed beneath the former circuit board to establish an interlayer connection.

12. A multi-layered semiconductor device as defined by claim 11, wherein at least one of the plurality of circuit boards incorporates a plurality of semiconductor chips therein.

13. A multi-layered semiconductor device as defined by claim 11, wherein every adjacent circuit board is bonded to another with an insulation adhesive.

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14. A multi-layered semiconductor device as defined by claim 11, wherein the semiconductor chip is accommodated in a through-hole formed in the insulation substrate of at least one of the plurality of circuit boards, and is electrically connected to the circuit of the circuit board by a beam lead bonding.

15. A multi-layered semiconductor device as defined by claim 11, wherein the semiconductor chip is accommodated in a through-hole formed in the insulation substrate of at least one of the plurality of circuit boards, and is electrically connected to the circuit of the circuit board and the semiconductor chip by a flip-chip connection.

16. A multi-layered semiconductor device as defined by claim 11, wherein the circuit on the circuit board is electrically connected, by means of a low melting point metal filled in a though-hole provided in the insulation substrate of the circuit board, to a circuit on an adjacent circuit bard to establish an interlayer connection.

17. A method for producing a multi-layered semiconductor device formed of a plurality of circuit boards layered together, each comprising an insulation substrate, a semiconductor chip incorporated in the substrate, a circuit formed on a surface of the substrate

and connected to the semiconductor chip, characterized in that a lead extending from the circuit on the circuit board is bonded in a through-hole provided in the insulation substrate of the circuit board to a circuit on another circuit board disposed beneath the former circuit board to establish an interlayer connection;

characterized in that the method comprises the steps: of individually testing the circuit boards and superposing the plurality of circuit boards on each other.

18. A method as defined by claim 17, wherein the circuit on the circuit board is electrically connected, by means of a low melting point metal filled in a though-hole provided in the insulation substrate of the circuit board, to a circuit on an adjacent circuit bard to establish an interlayer connection.

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